Docket No. 200308565-1

Amendments to the Claims:

Status of Claims:

Claims 1 - 44 are pending for examination.

Claims 1, 17, 29, 35, 37, 38, 44 are in independent form.

1. (Original) A system comprising:

a memory mapping logic configured to provide access to memory locations, where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location; and

a memory quality assurance logic operably connected to the memory mapping logic, where the memory quality assurance logic is configured to:

control copying contents between a first memory location and a second memory location;

reconfigure the memory mapping logic so that memory accessing operations intended for the first memory location are directed to the second memory location; and

initiate memory testing of the first memory location.

2. (Original) The system of claim 1, where the memory mapping logic includes a crossbar.

3. (Original) The system of claim 1, where the memory mapping logic includes one or more address translation tables.

4. (Original) The system of claim 1, where the memory quality assurance logic is configured to select the first memory location by one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method.

5. (Original) The system of claim 1, where the memory quality assurance logic is configured to selectively logically remove the first memory location from a first set of memory by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location.

6. (Original) The system of claim 1, where the memory quality assurance logic is configured to selectively logically replace the first memory location with the second memory location by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location.

7. (Original) The system of claim 1, where the memory quality assurance logic is configured to selectively logically replace the first memory location with another memory location from a first set of memory by reconfiguring the memory mapping logic based, at least in part, on a result from the memory testing of the first memory location.

8. (Original) The system of claim 1, where the memory quality assurance logic is configured to initiate memory testing of the first memory location by sending one or more signals to a memory testing logic.

9. (Original) The system of claim 1, where the memory quality assurance logic is configured to initiate memory testing of the first memory location by sending one or more signals to an onboard memory testing logic, where the onboard memory testing logic is physically connected to the first memory location.

10. (Original) The system of claim 1, where the memory quality assurance logic selects the second memory location.

11. (Original) The system of claim 1, where the memory quality assurance logic includes one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data.

12. (Original) The system of claim 1, where the memory quality assurance logic is operably connected to one or more data stores configured to store one or more of, a memory freshness

data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data.

13. (Original) The system of claim 1, where the second memory location is located in internal memory of the memory mapping logic.

14. (Original) The system of claim 1, where the second memory location is located in internal memory of the memory quality assurance logic.

15. (Original) The system of claim 1, where the second memory location is physically connected to the first memory location.

16. (Original) The system of claim 1, where the memory quality assurance logic is configured to select the second memory location.

17. (Original) A method comprising:

selectively copying contents of a first memory location to a second memory location;

logically replacing the first memory location with the second memory location; and

initiating memory testing of the first memory location without an operating system interaction.

18. (Original) The method of claim 17, where access to the contents of the first memory location as copied to the second memory location can continue concurrently with the memory testing.

19. (Original) The method of claim 17, where the memory testing of the first memory location can continue without consuming a non-memory operating system resource.

20. (Original) The method of claim 17, comprising identifying the first memory location by one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method.

21. (Original) The method of claim 17, where the first memory location is logically replaced by the second memory location by reconfiguring address resolving means.

22. (Original) The method of claim 17, comprising selectively logically removing the first memory location from a first set of memory.

23. (Original) The method of claim 17, comprising selectively logically replacing the first memory location with a third memory location, where the first memory location and the third memory location are physically located in the same memory apparatus.

24. (Original) The method of claim 17, comprising providing a report concerning a quality of the first memory location, where the report is based, at least in part, on the testing of the first memory location.

25. (Original) The method of claim 17, comprising storing a quality data associated with the quality of the first memory location, where the quality data is based, at least in part, on the testing of the first memory location.

26. (Original) The method of claim 17, where testing the first memory location includes two or more test methods.

27. (Original) The method of claim 17, where the first memory location can be tested by one or more of, a parity test, an electrical test, a striping test, a marching one test, a marching zero test, and a pattern test.

28. (Original) The method of claim 17, comprising selecting the second memory location to logically replace the first memory location.

29. (Original) A system, comprising:

a processor;

a memory operably connected to the processor, where the processor can access the memory;

a memory mapping logic configured to provide access to memory locations in the memory, where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location; and

a memory quality assurance logic operably connected to the memory mapping logic, where the memory quality assurance logic is configured to:

control copying contents of a first memory location between a second memory location;

reconfigure the memory mapping logic so that memory accessing operations intended for the first memory location are directed to the second memory location; and

initiate memory testing of the first memory location.

30. (Original) The system of claim 29, where the system is embedded in a computer.

31. (Original) The system of claim 29, where the system is embedded in an image forming device.

32. (Original) The system of claim 29, where the memory quality assurance logic includes one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data.

33. (Original) The system of claim 29, where the memory quality assurance logic is operably connected to one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data.

34. (Original) The system of claim 29, comprising a memory location selection logic configured to select the first memory location and the second memory location.

35. (Original) A computer-readable medium storing processor executable instructions operable to perform a method, the method comprising:

selecting a first memory location to test from a first set of memory;

selectively copying contents of the first memory location to a second memory location;

logically replacing the first memory location with the second memory location; and

initiating testing of the first memory location.

36. (Original) The computer-readable medium of claim 35, where the method comprises logically replacing the first memory location with the second memory location by reconfiguring address resolving means.

37. (Original) A system comprising:

means for logically replacing a testable memory location with a replacement memory location, where the means for logically replacing operates without interacting with an operating system;

means for testing the testable memory location, where the means for testing operates without interacting with an operating system; and

means for selectively logically removing the testable memory location from a set of memory based, at least in part, on a result of testing the testable memory location, where the means for selectively logically removing the testable memory location operates without interacting with an operating system.

38. (Original) An operating system transparent system for on-the-fly memory testing, comprising:

a memory location identifying logic configured to identify a target memory location and a replacement memory location;

a programmable memory address resolving logic configured to provide access to the target memory location and the replacement memory location; and

a test controlling logic operably connected to the programmable memory address resolving logic, the test controlling logic configured to selectively program the programmable

memory address resolving logic to divert memory accesses from the target memory location to the replacement memory location and to initiate testing of the target memory location,

where the memory location identifying logic, the programmable memory address resolving logic, and the test controlling logic do not consume operating system resources.

39. (Original) The system of claim 38, where the memory location identifying logic is configured to identify a target memory location using one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method.

40. (Original) The system of claim 38, where the programmable memory address resolving logic includes one or more of, a crossbar and an address translation table.

41. (Original) The system of claim 38, where the test controlling logic is also configured to selectively reprogram the programmable memory address resolving logic to stop diverting memory accesses from the target memory location to the replacement memory location.

42. (Original) The system of claim 38, where the test controlling logic is also configured to logically remove the target memory location from a pool of memory available to operating system instances without requiring an operating system instance to halt execution.

43. (Original) The system of claim 42, where the test controlling logic logically removes the target memory location from the pool of memory by reprogramming the programmable memory address resolving logic.

44. (Original) An operating system transparent method for on-the-fly memory testing, comprising:

identifying a test memory location and a mirroring memory location;

mirroring the test memory location to the mirroring memory location;

selectively reconfiguring memory accessing operations so that memory accesses originating in an operating system instance that are addressed to the test memory location are redirected to the mirroring memory location; and

testing the test memory location without disrupting an operating system instance.